

IN THE CLAIMS

Please amend the claims as follows:

1. - 9. (Canceled)

10. (Currently amended) A processor comprising:

a processor pipeline to output branch instruction addresses;

a branch target buffer responsive to the branch instruction addresses, wherein the branch target buffer comprises branch target buffer records to map branch instruction addresses to branch target addresses associated with an entry location of a first code region, wherein the branch target buffer records comprise confidence counters to track a number of times branches associated with the branch target addresses are taken; and

a presbyopic target buffer responsive to the branch target buffer, wherein the presbyopic target buffer comprises presbyopic target buffer records to map ~~branch target addresses to subsequent branch target addresses~~ the entry location of the first code region to an entry location of a second code region;

a cache memory to retrieve the instructions at the branch target addresses and the instructions at the subsequent branch target addresses;

a fetch buffer to receive the instructions at the branch target addresses;

a prefetch stream buffer to receive the instructions at the subsequent branch target addresses.

11. (Canceled)

12. (Original) The processor of claim 10 wherein the presbyopic target buffer is configured to be recursively searched to predict a plurality of subsequent branch target addresses.

13. (Original) The processor of claim 10 wherein the presbyopic target buffer implements skip-adjacent mapping.

14. (Original) The processor of claim 10 wherein a complete branch target address is specified by a fixed number of bits, and the presbyopic target buffer includes mapping records that specify branch target addresses using less than the fixed number of bits.

15. - 25. (Canceled)

26. (Currently amended) A method comprising:

processing instructions in a processor pipeline, wherein the processing is to output branch instruction addresses

in a branch target buffer that maps the branch instruction addresses to block entry addresses associated with entry locations of first code regions, searching for a branch target buffer record having a branch instruction address that matches a current instruction address;

after the branch target buffer record is found, incrementing a confidence counter in the branch target buffer record and searching a presbyopic target buffer that maps ~~block entry addresses to subsequent block entry addresses~~ entry locations of the first code region to entry locations of a second code region for a presbyopic target buffer record having a block entry address matching the branch target buffer record; and

after the presbyopic target buffer record is found, incrementing a confidence counter in the presbyopic target buffer record and prefetching instructions beginning at ~~a subsequent block entry address~~ the entry location of the second code region included in the presbyopic target buffer record.

27. (Original) The method of claim 26 wherein prefetching comprises entering instructions into a stream buffer, the stream buffer having a coloring field for each instruction entered.

28. (Previously Presented) The method of claim 26 further comprising:
searching the presbyopic target buffer recursively; and

for each matching record found in the presbyopic target buffer, each matching record having a corresponding subsequent block entry address, prefetching instructions from each of the corresponding subsequent block entry addresses.

29. (Original) The method of claim 28 wherein prefetching comprises:

entering instructions into a stream buffer, the stream buffer having a coloring field for each instruction entered; and

assigning a different color to instructions fetched from different subsequent block entry addresses.

30. (Original) The method of claim 29 wherein each recursive search represents a predicted branch, the method further comprising flushing from the stream buffer instructions prefetched as a result of a mispredicted branch.

31. (Previously presented) The processor of claim 10, wherein the presbyopic target buffer records comprise confidence counters to track a number of times branches associated with the subsequent branch target addresses are taken.